

ABSTRACT OF THE DISCLOSURE

A combination wafer is manufactured by (i) forming a plurality of alternating dielectric and metal layers, (ii) forming a guard ring trench in the layers, (iii) forming a guard ring layer in the guard ring trench, and then repeating (i), (ii) with a slightly wider guard ring trench, and (iii). A number of layers are thus simultaneously etched and lined with a guard ring layer, but the number of layers is not so large so as to cause lithographic problems that may occur when a deep, narrow guard ring trench is formed. An upper one of the layers that are patterned is always made of silicon dioxide, which includes less carbon than lower polymer layers and allows for a carbon mask to be formed and be easily removed. The slightly wider guard ring trench each time the process is repeated overcomes lithographic alignment problems that may occur when the guard ring trenches are exactly the same size. Subsequent guard ring layers are partially formed on one another, and provide a moisture seal. The guard ring layers are formed at the same time when vias are formed that are connected to electronic elements.